FORM PTO-1449 (Modified)	ATTY. DOCKET NO.: A0312/7400	SERIAL NO.: 09/575,562
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	APPLICANT: Haurie, et al.	
	FILING DATE: May 21, 2000	GROUP: ~~2819~~ 2818

U.S. PATENT DOCUMENTS

Exam Init	Ref Des	Document No.	Date	Name	Class	Sub Class	FILING DATE If Appropriate
TP		5,404,142	04.04.95	Adams, et al.	341	144	
TP		5,412,387	05.02.95	Vincelette, et al.	341	150	
TP		5,969,657	10.19.99	Dempsey, et al.	341	145	
TP		5,977,899	11.02.99	Adams	341	145	

FOREIGN PATENT DOCUMENTS

		Country & Doc. No. (11)	Pub. Date (43)		Class	Sub Class	Translation Yes	Translation No

OTHER ART
(Including Author, Title, Date, Pertinent Pages, Publication, Etc.)

TP		1	Yoshizawa, et al. Novel Design Techniques for High-Linearity MOSFET-Only Switched-Capacitor Circuits, 1996 Symposium on VLSI Circuits Digest of Technical Papers, pp 152-153
TP		2	Wang, et al., A Quasi-Passive CMOS Pipeline D/A Converter, IEEE Journal of Solid-State Circuits Vol. 24, No. 6, December 1989, pp 1752-1755
TP		3	Wang, et al., A Quasi-Passive CMOS Pipeline D/A Converter, IEEE 1988 Custom Integrated Circuits Conference, 1988, pp 18.1.1-18.1.4
TP		4	Temes, et al., Novel Pipeline Data Converters, ISCAS'88, pp 1943-1946
TP		5	Yoshizawa, et al. MOSFET-Only Switched-Capacitor Circuits in Digital CMOS Technology, IEEE Journal of Solid-State Circuits, Vol. 34, No. 6, June 1999, pp 734-747
TP		6	Kwan, Tom, et al., "A Stereo Multibit Sigma-Delta DAC with Asynchronous Master-Clock Interface", IEEE Journal of Solid-State Circuits, Vol. 31, No. 12, Dec. 1996, pp. 1881-1887

EXAMINER	Trong Phan	DATE CONSIDERED	7/6/01

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered.
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